



AHB matrix - Verilog IP Core

FEATURES

- Fully compliant with AMBA 2.0 specification
- Highly configurable to support a broad range of system architecture
- Configuration of data bus widths of 32, 64 or 128 bits
- Address, data bus widths and endianness must be the same for all layers
- Support for single and all types of burst transfers
- Support for full AHB (split, retry and error) and AHB lite
- Support 1 to 16 layers
- Support 1 to 16 masters
- Support 1 to 64 slaves
- Configurable pipeline architecture with one cycle latency or no pipeline architecture with zero latency. Enables user optimization for low latency or high frequency
- Fixed, programmable and round-robin priority mechanism
- Integrated page table for virtual addressing
- Map slave response to relevant layer
- Address re-mapping for ROM/RAM swapping
- Support one clock domain for all masters and slaves
- Configuration registers are using APB bus
- Fully synthesizable
- Fully synchronous design
- DFT ready
- Power optimized
- Silicon proven both in ASIC and FPGA technologies

INTRODUCTION

The AMBA Advanced High-performance Bus is tailored for high-performance, high-clock frequency system buses.

The AHB acts as the high-performance system backbone bus. AHB supports the efficient connection of processors, on-chip memories, on chip peripheral and off-chip external peripheral functions. AHB is also specified to ensure ease of use in efficient design flow using synthesis and automated test techniques.

Inomize's AHB matrix soft IP core complies with the **AMBA 2.0** specification. The core is a highly configurable multi-layer AHB matrix bus. It supports 1 to 16 masters and 1 to 64 slaves with 1 to 16 layers. It is the most flexible and generic IP of its kind. This makes it suitable to support various system types, from the simplest to the most complicated. It is also tailored to have the best performance in terms of latency, throughput and bus frequency.

The core is provided with generation script so that the user can very easily select the required configuration and generate the corresponding verilog code.

The configuration is selected pre-synthesis (RTL).

Three types of priority mechanisms are included to be compatible with various system needs.

Clocks rates

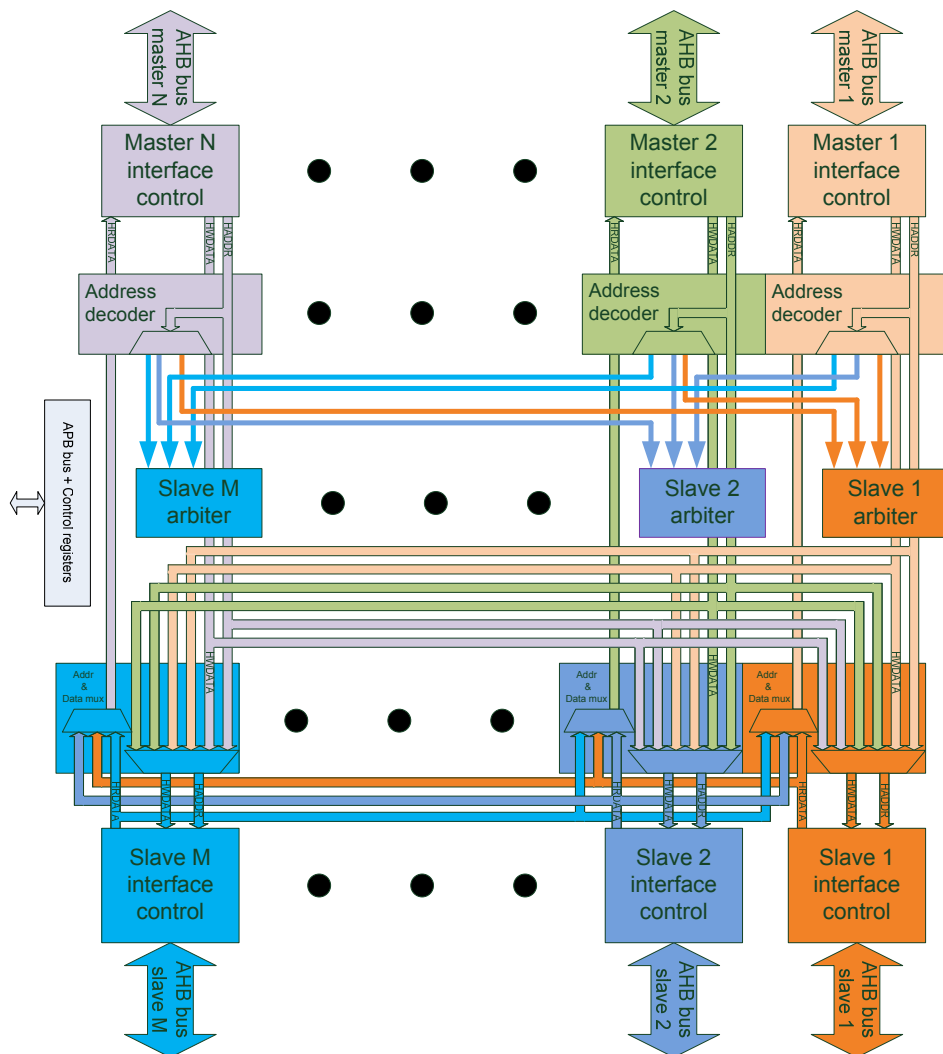
The AHB matrix can support 0 to 300MHz of bus frequency. It is a single clock domain design.

System interface

The AHB matrix supports full AHB and AHB lite and APB bus for the configuration registers.

The AHB matrix support transfer sizes of 8, 16, 32, 64 and 128 bits

FUNCTIONAL BLOCK DIAGRAM



The AHB matrix main blocks are:

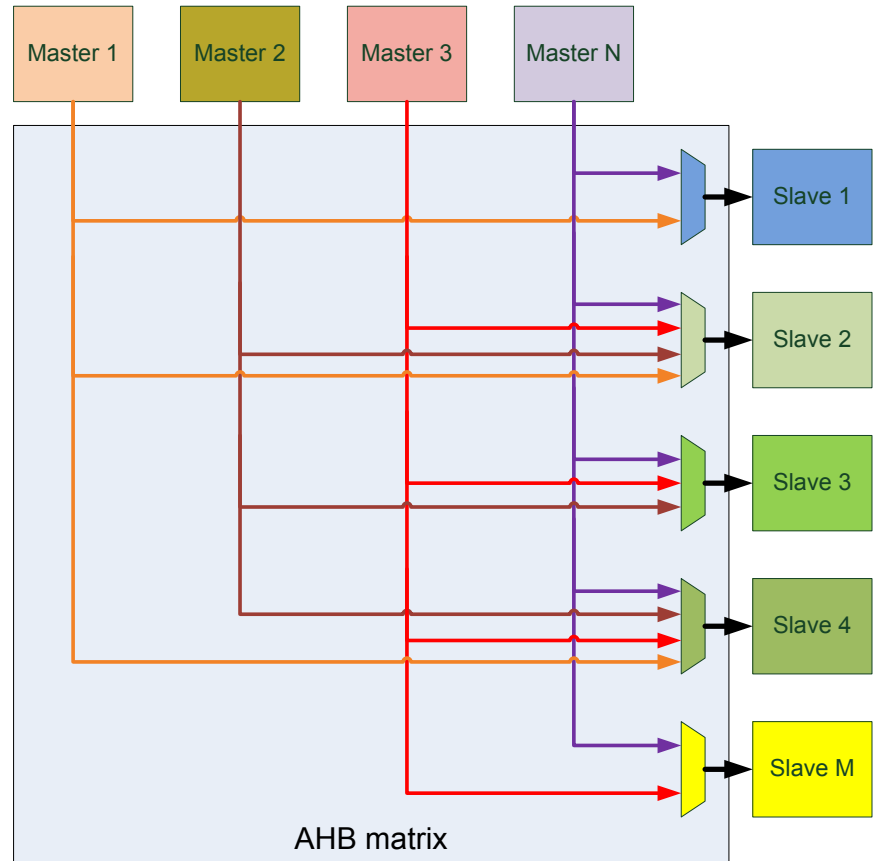
- **Master interface control:**
Handles the master interface signals to the AHB matrix. This block makes sure the master "believes" that it is a single master in the system.
- **Address decoder:**
This block is doing the address decoding and generate an internal select controls for the relevant slave. It also returns ERROR response for illegal addresses
- **Slave arbiter:**
The arbiter is receiving all the address decoding request and performing the arbitration scheme according to a pre-determined architecture. It support fixed, programmable and round-robin architectures. The arbitration is done without any wait states so if no other master is accessing the slave, the master is connected to the slave at the same cycle.
- **Address and data muxing:**
The address and data coming from the master interface is muxed towards the corresponding slave interface while the data coming from the slave bus is muxed towards the corresponding master bus
- **Slave interface control:**
Handles the AHB save interface signals from the AHB matrix

- Silicon and FPGA proven
- Highly configurable
- Performance optimized

BENEFITS

- Highly configurable to support any SoC requirement
- Easy for configuration
- Zero latency and wait-states
- Integrated "Auto increment" to support high speed bus requirement
- Glue-less integration with Any AHB master or slave
- No internal memory
- Extremely small gate count
- Power optimized
- Silicon and FPGA proven in many configurations

SYSTEM BUS DESCRIPTION



DELIVERIES



- Synthesizable RTL design in Verilog
- Verilog test integration environment
- Technical documents (User guide, Architecture, detailed design and integration guidelines)
- Synthesis and STA scripts

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