DMAC100 - Verilog DMA Controller IP Core

FEATURES

- Complies with AMBA Advanced High Performance Busses – AHB or AXI
- Supports 1-10 DMA channels
- Support 1-32 peripherals
- Two AHB Bus masters for data transfer
- One AHB Bus slave for internal programming
- Single clock domain architecture based on master system clock
- Supports maximal transfer size of 64KByte (16KWord). Transfer size can be of any size within this limit (not restricted to power of 2)
- Supports burst sizes of 1, 4, 8 and 16
- Supports transfer data width of 8bit (byte), 16bit (half word), 32bit (word) and 64bit (double word)
- Supports Little-endian (default) and Big-endian
- Each peripheral can use a burst requests or a single requests
- Supports Scatter/Gather operation through Liked List – keeps continuity of DMA operation without the need of new CPU programming
- Two independent FIFO buffers that also support double buffer operation
- Supports fixed priority or round robin arbitration
- Supports four types of data transfer –
  - Memory to Memory
  - Memory to Peripheral
  - Peripheral to Memory
  - Peripheral to Peripheral
- Incrementing and non-incrementing addresses for source and for destination
- Can be halted or aborted during data transfer
- Generates transfer complete, time out and transfer error Interrupt
- Masking option for all channels interrupts
- Raw interrupts status

INTRODUCTION

The DMAC100 is used to transfer large amounts of data between memories and peripherals using AHB/AXI buses in SoC environment in order to reduce CPU overhead for data transfers.

The DMAC100 has one Bus Slave interface for programming its internal registers and one or two bus master interfaces for data transfer.

The DMAC100 has parameterized number of channels, each channel transfers data between one or two slaves (memory or peripheral). The direction, bus master, data width, transfer size, burst size and endiannity are configurable.

Each bus master interface has its own channels requests arbiter. The arbitration scheme is programmable and can be fixed priority arbitration or round robin arbitration.

The DMAC100 supports double buffered operation using two read-in write-out 64bits wide FIFOs. Each bus master interface has bidirectional access to each FIFO to achieve best system bus.

The DMAC100 supports a parameterized number of DMA peripheral requestors which can be routed to each one of the DMAC100 channels.

An individually maskable interrupt is generated for transfer complete, time out and error. All channels interrupts are stored in status registers and can be accessed before and after masking.

All DMAC100 channels perform Scatter/gather operation through linked list Items (LLI). The first LLI is programmed into each DMAC channel.

The DMAC100 has single clock domain architecture.

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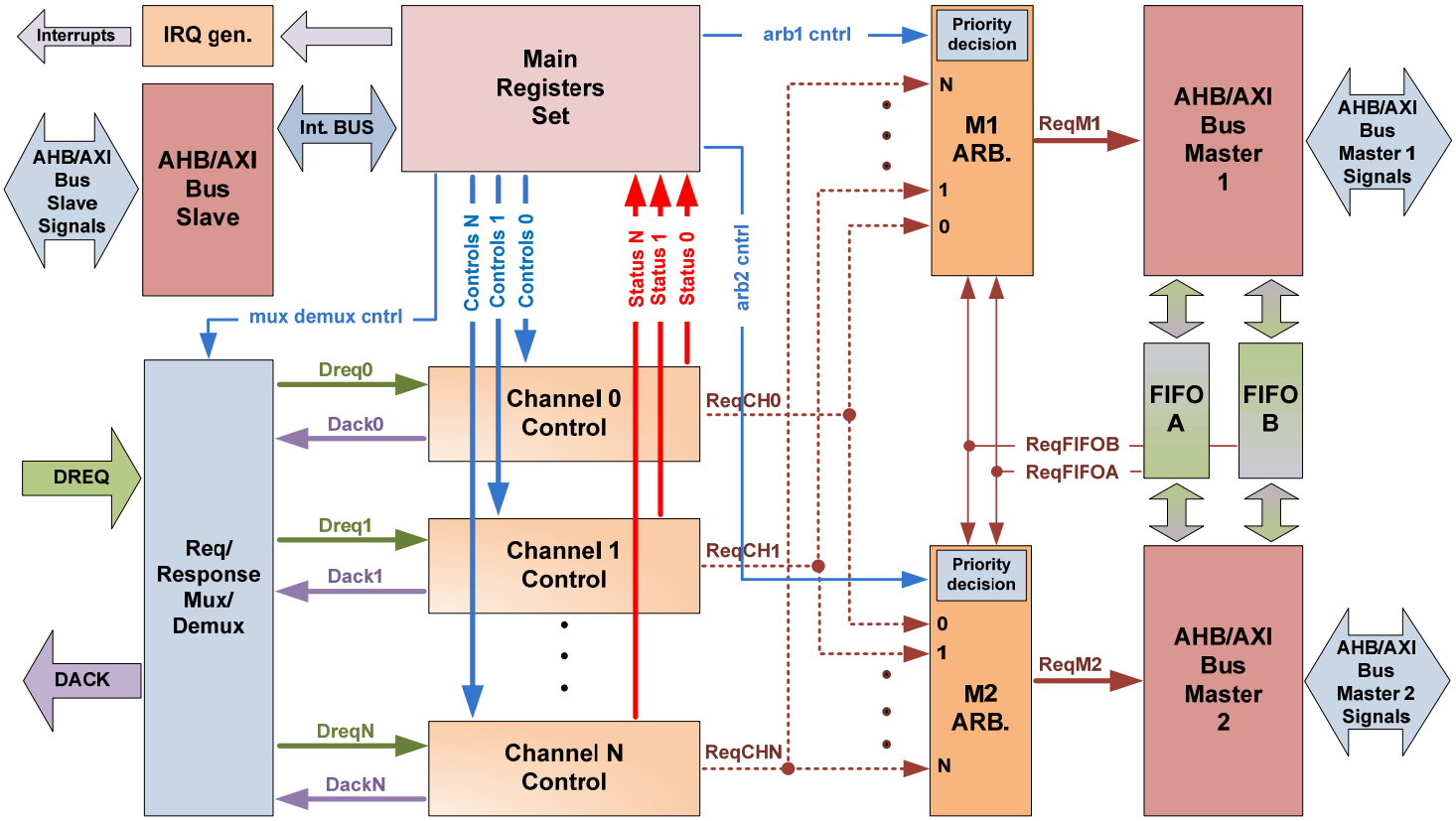
FUNCTIONAL BLOCK DIAGRAM



The DMA main blocks are:

- AHB/AXI Bus Master 1/2:
  The DMAC100 holds one or two bus master interfaces for data transfer. Both masters can work independently or together. The masters support back to back transfers.

- AHB/AXI Bus Slave and main register set:
  This block is a memory mapped register set used to control the operation of the DMAC100. The registers store the controls and the interrupts information of every channel.

- Response mux/De-mux:
  This block connects each DMA peripheral to each DMA channel in terms of requests and acknowledge signals.

- DMA Channels:
  Main DMA data transfer control block. Each DMA channel is individually configured with parameters which are used to control data transfer between memories and peripherals.

- Master Arbiter 1/2:
  DMA channels arbitration block. This block is used to select which channel has the highest priority for data transfer. Each bus master hold one arbiter which can be programmed to either fixed priority or Round Robin arbitration methods.

- FIFO A/B:
  The DMAC100 data FIFOs are 64bits wide and used by the bus masters in data transfer process. Both masters can access both FIFOs for read or write operations. The FIFOs depth is configurable during compilation.

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DMAC100 - Verilog DMA controller IP Core

- *Optimized for high speed and high performance*
- *Highly configurable*

BENEFITS

- Highly parameterized to support any area to performance tradeoff
- Very smart DMA channels logic provides the ability to transfer any size of data within a predefined limit
- Capable of transfer data in several widths (8, 16, 32 and 64bit)
- Using two AHB/AXI bus masters which allows simultaneously reads and writes transaction (performing back to back transfer to save bus cycles)
- Extremely efficient system bus operation
- Power optimization
- Timeout indication for bus usage analysis and troubleshooting
- Glue-less integration
- Extremely small gate count without internal memories

DELIVERIES

- Synthesizable RTL design in Verilog
- Verilog test integration environment
- Technical documents (User guide and integration guidelines)
- Synthesis and STA scripts

PROGRAMMABLE OPTIONS

- DMA enable/disable
- DMA interrupts masking option
- DMA arbitration type
- DMA master selection for source and destination
- DMA masters Endiannity
- Channel's enable/disable
- Channel's source and destination addresses
- Channel's source and destination address access mode
- Channel's data transfer direction
- Channel's transfer (message) size in bytes
- Channel's maximal burst size in bytes
- Channel's maximal data width
- Channel's LLI first address
- Channel's interrupts enable/disable

PARAMETRIZED OPTIONS

- Depth of FIFO A and B
- Number of DMA channels
- Number of DMA requestors
- One or two bus masters
- Number of DMA channels (1 to 10)
- Number of peripherals (1 to 32)

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