



SPI100 - Verilog SPI IP Core

FEATURES

- Full-duplex, RX only or TX only operation
- Four wire bus — RX and TX data, clock, select
- Supports being slave in multi-slave environment or being master over parameterized number of slaves
- Programmable automatic header/pattern detection
- Memory mapped AHB/APB interface
- Option to use an independent reference clock to decouple AHB/APB clock from SPI clock
- Allows flexible clock ratios, including SPI serial bit clock frequency of x2 of the AHB clock frequency for 8bits frames, x4 for 16bits frames and x8 for 32bits frames
- Supports AMBA AHB and/or APB bus types
- Master or slave SPI modes of operation
- Motorola or TI protocol
- Programmable polarity and clock phase
- Supports serial data width of 8/16/32 bits
- AHB can access one sample each time or reduce AHB bandwidth when data width is 8bits or 16bits by accessing multiple samples.
- Programmable master mode clock frequencies
- FIFO level status monitoring via software, interrupt or DMA HW handshake for flow control
- Programmable timeout in slave mode when RX FIFO is not empty and no transaction is detected
- Programmable serial bit order LSB or MSB first
- Parameterized number of chip selects and number of data in pins

INTRODUCTION

The Serial Peripheral Interface (SPI100) provides full-duplex, synchronous, digital, serial communication between master and slave, over a 4 wire bus.

It can be connected to any peripheral supporting Motorola SPI synchronous serial interface or TI synchronous serial frame format.

The Motorola SPI uses one serial clock wire, one active low chip select wire and one data wire in each direction. The chip select is active around one or more consecutive data transfers and the clock can be operated in one of four modes of clock polarity and clock phase compared to the data. Multiple chip selects can be used by a single master to control many slaves.

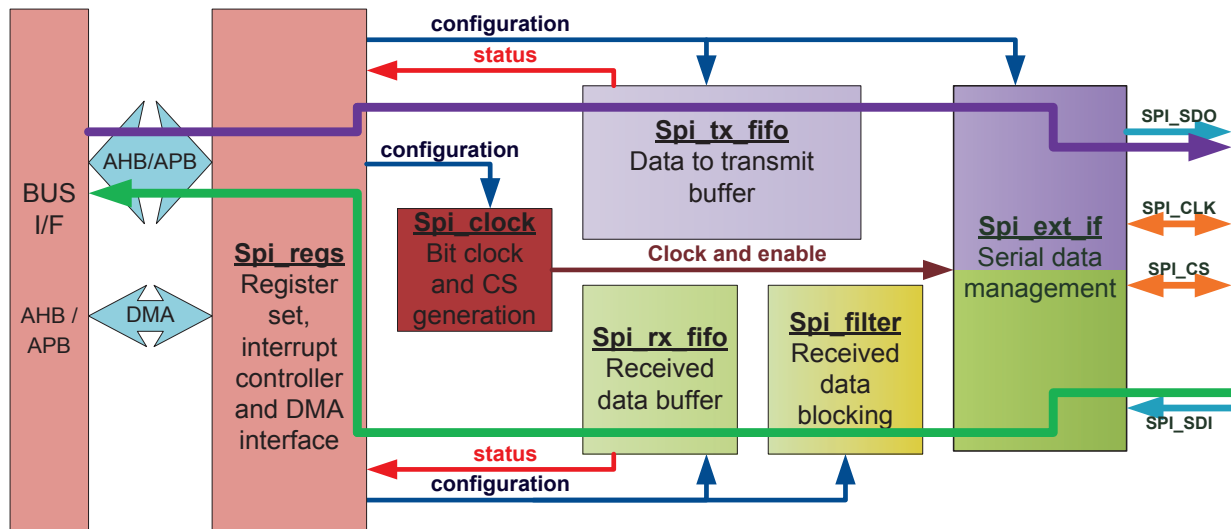
The TI SPI uses one serial clock wire, one active high chip select wire and one data wire in each direction. The chip select is active for one cycle before the first data bit. In consecutive data transfers the chip select is raised for one cycle before the start of each new frame (during the last cycle of the current frame).

The SPI100 is AMBA AHB and/or APB slave for control, for status and for high bandwidth data transfer. The SPI100 can work with very fast serial bit clock over the interface in any rate up to eight times the frequency of the AHB or APB clock. In slave mode, the bit clock is received over the bus and in master mode the clock is a division of the AHB clock or of a dedicated system clock.

The data flow can be CPU controlled by interrupts of various FIFO statuses or DMA controlled by dedicated DMA HW handshake for efficient flow control.

- Optimized for high speed
- Highly configurable

FUNCTIONAL BLOCK DIAGRAM



BENEFITS

- Option for very high bit rate with low AHB frequency
- High bandwidth AHB interface for optimized DMA operation
- Automatic header detection
- Option to work in half duplex: only RX without the need to send padding data on TX or only TX without having to clear RX FIFO all the time
- Timeout indication in slave mode when RX FIFO is not empty and no new transaction is detected
- Glue-less integration
- Extremely small gate count without internal memories



DELIVERIES

- Synthesizable RTL design in Verilog
- Verilog test integration environment
- Technical documents (User guide and integration guidelines)
- Synthesis and STA scripts

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SPI100 – REV1.5

SPI MAIN BLOCKS

- **Spi_regs:**
This block is the configuration register file, the interrupt generator and the DMA interface control.
- **Spi_clock:**
This block generates the chip select and the serial clock in master mode
- **Spi_ext_if:**
This block does parallel to serial on transmit data and serial to parallel on receive data according to serial bus bit clock
- **Spi_filter:**
received data filtering until a synchronization pattern is detected
- **Spi_Spi_rx_fifo:**
Received data buffering between serial bus and AHB/APB. Fullness of the FIFO is used for various interrupts and DMA controls
- **Spi_Spi_tx_fifo:**
Transmitted data buffering between AHB/APB and serial bus. Fullness of the FIFO is used for various interrupts and DMA controls