UNI100 - Verilog UniPro IP Core

MOBILE INDUSTRY PROCESSOR INTERFACE

FEATURES

- Compliant to ***UniPro*** Specification version 1.1
- Compliant to ***MIPI D-PHY*** Specification version 0.9
- System interface using one or two system busses each can be bus master or bus slave (Bus types options: AXI, AHB, BVCI)

L4:

- Configurable number of Cports for RX and for TX – up to 2048 Cports in each direction
- Message segmentation and composition of segments (TX) and segments decomposition and reassembly to messages (RX)
- End to end flow control. TX path can block outgoing data on specific Cport and RX path can drop messages not picked fast enough by DMA
- Support of 2 traffic classes with priority

L3:

- Generation of device ID (TX)
- Discarding packets of all but the requested device ID (RX)
- Configuration parameters: source and destination device ID, layer bypass enable

L2:

- Frame composition (TX) and decomposition (RX) of variable lengths
- Full support for frame preemption in TX and in RX
- Flow control with credit information
- Support of 2 traffic classes with priority
- CRC generation (TX) and verification (RX)
- Frame retransmission in case of error or timeout
- Autonomous acknowledgment for all received frames (ACK or NAC)

L1.5:

- Support of 1 to 4 PHY lanes with data transfer rate of up to 800Mbps per lane and 3.2 Gbps total
- Generation and removal of IDLE symbols when needed
- Support of all MIPI UniPro defined power management operating modes
- Link startup for initialization and re-initialization of the PHY TX path
- Optional PHY encoding (TX) and decoding (RX)

INTRODUCTION

The MIPI Alliance Standard for Unified Protocol (UniPro) defines a layered protocol for interconnecting devices and components within mobile systems such as mobile phones, handheld computers, digital cameras, and multimedia devices. UniPro allows these devices and components to exchange data at high data rates, with low pin counts and at low energy per transferred bit. UniPro is applicable to a wide range of component types such as application processors, co-processors, modems, etc. and to different types of data traffic such as control messages, bulk data transfer, packetized streaming. The standard defines the protocol used to transfer data between devices that implement the UniPro. This includes definitions of data structures, such as Packets and Frames, used to convey information across the network. In addition, flow control, error handling, power and state management, and connection services are also within the standard.

mipi alliance member

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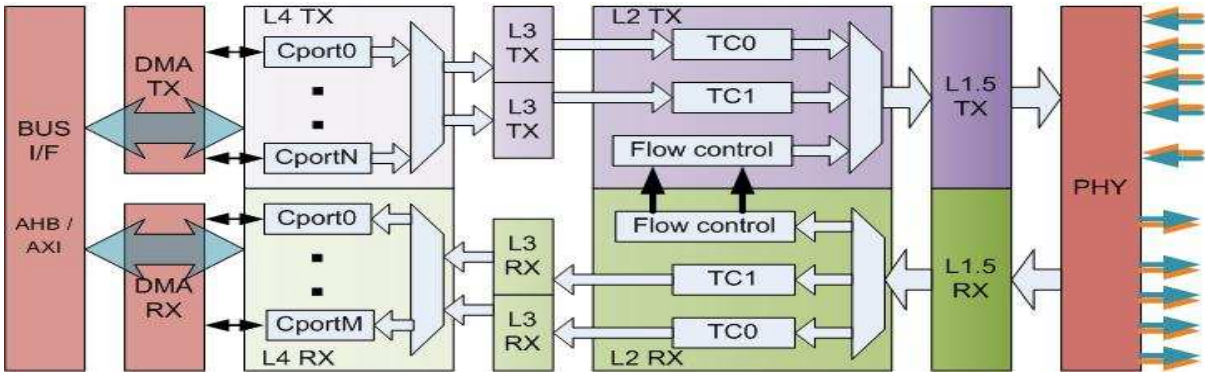
FUNCTIONAL BLOCK DIAGRAM



The UNI100 Core main blocks are:

- System bus:

  This block connects the L4 Cports to the system. This block add the option for internal DMA or can use external DMA engine to handle all data transfers from the system memory to L4.

- L4TX:

  This block supports the transport layer protocol. The outgoing messages are segmented and the segments are read by L2TX. Available segments information (segment parameters, RAM location) is passed to the L3TX.

- L3TX:

  This block supports all of the network layer protocol. It forwards all L4TX parameters along with destination device ID towards L2TX.

- L2TX:

  This block supports all of the data link layer protocol. Segments from L4TX are packed and framed according to configuration arriving from L3TX. The frames are stored in TX RAM to be sent to L1.5TX. The TX RAM is also used as the retransmit buffer. All flow control operations (credits, ACK, NAC) are done automatically.

- L1.5TX:

  This block supports the PHY adapter layer protocol. The block receives symbols from L2TX and passes them towards 1 to 4 PHY lanes. The link startup protocol support is also part of this block.

- L1.5RX:

  This block supports the PHY adapter layer protocol. The block receives symbols from 1 to 4 PHY lanes, multiplex the symbols to one stream, remove IDLE symbols and sends them towards L2RX.

- L2RX:

  This block supports all of the data link layer protocol. Symbols from L1.5RX are decoded, built into frames, CRC checked and stored in RX RAM. According to header correctness and CRC, ACK or NAC for each frame are sent automatically towards L2TX. Acknowledged frames are sent towards L3RX.

- L3RX:

  This block supports all of the network layer protocol. It filters L2RX packets according to device ID and sends the segments towards L4RX.

- L4RX:

  This block supports the transport layer protocol. The incoming segments from L3RX are demultiplexed into Cports and stored in incoming messages RAM. Available segments are copied by DMA to system memory where they are used to build full messages.

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MOBILE INDUSTRY PROCESSOR INTERFACE

- ***Easy area Vs. performance tradeoff***
- ***Power & performance optimized***
- ***Highly configurable***

BENEFITS

- Highly parameterized to support any area to performance tradeoff
- Extremely efficient pipeline – throughput is only limited by the speed of the system bus or the PHY bit rate
- System interface using one or two system busses each can be bus master or bus slave. Bus slave interfaces the system using DMA requests
- Glue-less integration with the subsystem and the D-PHY
- Single controller can support operation with two PHYs at the same time if each is used to transfer messages only in one direction
- All used memories are single port RAM with 64 bits width. No dual port memories are needed
- Power optimization

DELIVERIES

- Synthesizable RTL design in Verilog
- Verilog test integration environment
- Technical documents (User guide, Architecture, detailed design and integration guidelines)
- Synthesis and STA scripts
- Sample Drivers

DESCRIPTION

Inomize UNI100 soft IP core complies with the ***UniPro*** specification version 1.1 and glue-less connected to the ***MIPI D-PHY*** . The core implements the PHY Adapter, Data Link, Network, and Transport Layers as defined by the standard. The core is highly parameterized to allow the user selection of the best ***area to performance tradeoff*** for the system. The parameters are selected pre-synthesis (RTL) and unused options don't cost silicon area.

Clocks rates

The controller uses two clocks: a system clock for the system interface and most of the controller's logic and a PHY clock.

The design is built in a way that the possible throughput is only limited by speed of the system bus or the PHY bit rate.

System interface

The system can access all the Cports through one or two external DMA controllers or through one or two internal DMA controllers.

The data transfer rate is the sum of all TX and RX transfers. Using one system bus multiplex both streams in time while using two distinct busses allowing each bus to transfer only one direction of data.

The UNI100 IP optionally include a TX DMA controller and a RX DMA controller. The 2 controllers can optionally be multiplexed to one bus master using an integrated bus arbiter. The supported bus types are AXI, AHB and BVCI

Number of Cports

Each Cport can handle one direction of messages streaming. Since each Cport is a DMA channel and needs RAM pointers and flow control state machine, extra area is used by each port. Only the required number of ports for RX and for TX can be selected.

Memories size

All used memories are 64 bits wide, single port synchronous memories working on the system bus clock. The depth of each memory can be selected to match exactly the needed performance.

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